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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,136	11/03/2003	Tomio Matsuzaki	03663/LH	3722

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/700,136	Applicant(s) MATSUZAKI ET AL.	
	Examiner Steven Loke	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,36 and 37* is/are pending in the application.

4a) Of the above claim(s) *5-11 and 17-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,12-16,36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 2, 3, 4, 36 and 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2, lines 2-4, the phrase "each said interconnection is formed on the bottom surface of the corresponding recess in the insulating film" is vague and indefinite if claim 1 discloses the at least one interconnection formed on the upper surface of the insulating film. Fig 1 only discloses the interconnection [8] is formed on the bottom surface of the recess [7] in the insulating film [5]. The interconnection [8] never formed on the upper surface of the insulating film in fig. 1.

Claim 3, lines 2-5, the phrase "each said recess in the insulating film has a pair of side surfaces, and a space is provided between each said at least one interconnection and the side surfaces of the at least one recess" is vague and indefinite if claim 1 discloses the at least one interconnection formed on the upper surface of the insulating film. Fig 1 only discloses said recess [7] in the insulating film [5] has a pair of side surfaces, and a space is provided between said interconnection [8] and the side surfaces of the recess. In addition, the interconnection [8] is formed on the bottom surface of the recess [7] in the insulating film [5]. The interconnection [8] never formed on the upper surface of the insulating film in fig. 1.

Claim 4, lines 9-10, the phrase "the interconnections" is unclear whether it is being referred to the "at least one interconnection" of claim 1.

Claim 36, lines 18-21, the phrase "each said recess in the insulating film has a pair of side surfaces, and a space is provided between each said at least one

interconnection and the side surfaces of the at least one recess" is vague and indefinite if lines 12-13 of claim 36 discloses the at least one interconnection formed on the upper surface of the insulating film. Fig 1 only discloses said recess [7] in the insulating film [5] has a pair of side surfaces, and a space is provided between said interconnection [8] and the side surfaces of the recess. In addition, the interconnection [8] is formed on the bottom surface of the recess [7] in the insulating film [5]. The interconnection [8] never formed on the upper surface of the insulating film in fig. 1.

Claim 37, lines 8-11, the phrase "the protective film has a plurality of recessed surfaces in the recesses which are lower than an upper surface of the protective film" is vague and indefinite. Fig. 1 discloses the protective film [5] has a plurality of recesses and each of the recesses has a recess surface which is lower than an upper surface of the protective film [5]. Claim 37 should be rewrite as "the protective film has a plurality of recesses and each of the recesses has a recess surface which is lower than an upper surface of the protective film".

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3, 4, 12, 13, 36 and 37 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kimura.

In regards to claim 1, Kimura shows all the elements of the claimed invention in fig. 1. It is a semiconductor device, comprising: a semiconductor substrate [21] having a plurality of connecting pads [22] on one surface; an insulating film [24a, 24b] which is formed of a single layer [24] and covers said one surface of the semiconductor substrate, and which includes: (i) a plurality of holes (the area where wires [23] are formed) extending through the insulating film, each of the holes corresponding to one of the connecting pads [22], and (ii) at least one recess (the area between layer [24b]) extending partially through the insulating film such that a bottom surface of the recess is depressed with respect to an upper surface of the insulating film in a direction of thickness of the insulating film; and at least one interconnection (the lower portion of layer [26]) formed on the upper surface of the insulating film, each said at least one interconnection being connected to a corresponding one of the connecting pads through a corresponding one of the holes in the insulating film.

In regards to claim 3, Kimura further discloses each said recess in the insulating film has a pair of side surfaces, and a space is provided between each said at least one interconnection and the side surfaces of the at least one recess.

In regards to claim 4, Kimura further discloses the at least one interconnection comprises a connecting pad (the lower portion of layer [26]), and the semiconductor device further comprises: a bump electrode (the middle portion of layer [26]) formed on the connecting pad portion, and an encapsulating film [25] formed around the bump electrode and on the insulating film [24b] and the interconnections.

In regards to claim 12, Kimura inherently discloses the insulating film [24] is made of an organic resin because it is well known in the art that resin is an organic material.

In regards to claim 13, Kimura further discloses the recess in the insulating film [24a, 24b] has a depth which is not less than a thickness of the interconnection.

In regards to claim 36, Kimura shows all the elements of the claimed invention in fig. 1. It is a semiconductor device, comprising: a semiconductor substrate [21] having a plurality of connecting pads [22] on one surface; an insulating film [24a, 24b] which covers said one surface of the semiconductor substrate, and which includes: (i) a plurality of holes (the area where wires [23] are formed) extending through the insulating film, each of the holes corresponding to one of the connecting pads [22], and (ii) at least one recess (the area between layer [24b]) extending partially through the insulating film such that a bottom surface of the recess is depressed with respect to an upper surface of the insulating film in a direction of thickness of the insulating film; and at least one interconnection (the lower portion of layer [26]) formed on the upper surface of the insulating film, each said at least one interconnection being connected to a corresponding one of the connecting pads through a corresponding one of the holes in the insulating film; each said recess in the insulating film [24b] has a pair of side surfaces, and a space is provided between each said at least one interconnection and the side surfaces of the at least one recess.

In regards to claim 37, Kimura shows all the elements of the claimed invention in fig. 1. It is a semiconductor device, comprising: a semiconductor substrate [21] having a plurality of connecting pads [22] on one surface; a protective film [24a, 24b] formed of a

single layer, said protective film including: (i) a plurality of holes (the area where wires [23] are formed) extending completely through the protective film, each of the holes corresponding to one of the connecting pads [22], and (ii) a plurality of recesses (the area between layer [24b]) extending partially through the protective film such that the protective film has a plurality of recessed surfaces in the recesses which are lower than an upper surface of the protective film in a thickness direction of the protective film; and interconnections (the lower portion of layer [26]) which are respectively connected to the connecting pads [22] through the holes in the protective film, and which are provided on the upper surface of the protective film.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura.

In regards to claim 14, Kimura differs from the claimed invention by not showing the insulating film has a thickness of 10 to 30 microns. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the insulating film has a thickness of 10 to 30 microns, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claim 15, Kimura differs from the claimed invention by not showing the recess has a depth of 5 to 15 microns. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the recess has a depth of 5 to 15 microns, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

In regards to claim 16, Kimura differs from the claimed invention by not showing a distance between a bottom surface of the insulating film and the bottom surface of the recess is not less than 1 micron. It would have been obvious to one having ordinary skill in the art at the time the invention was made for a distance between a bottom surface of the insulating film and the bottom surface of the recess is not less than 1 micron, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sakamoto et al.

In regards to claim 1, Sakamoto et al. show all the elements of the claimed invention in figs. 10A and 10B. It is a semiconductor device, comprising: a semiconductor

substrate [12] having a plurality of connecting pads (the lower portion of layer SD) on one surface; an insulating film (the under-fill material AF and [14]) (paragraphs [0052] and [0053]) which is formed of a single layer and covers said one surface of the semiconductor substrate, and which includes: (i) a plurality of holes (the area where the upper portion of layer SD is formed) extending through the insulating film, each of the holes corresponding to one of the connecting pads, and (ii) at least one recess (the area adjacent layer [14]) extending partially through the insulating film such that a bottom surface of the recess is depressed with respect to an upper surface of the insulating film (the top surface of layer [14]) in a direction of thickness of the insulating film; and at least one interconnection [23] formed on the bottom surface of a corresponding said at least one recess, each said at least one interconnection being connected to a corresponding one of the connecting pads through a corresponding one of the holes in the insulating film.

In regards to claim 2, Sakamoto et al. further disclose each said interconnection [23] is formed on the bottom surface of the corresponding recess in the insulating film

8. Applicant's arguments with respect to claims 1, 2, 4 and 12-16 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
July 10, 2005

Steven Loke
Primary Examiner
Steven Loke